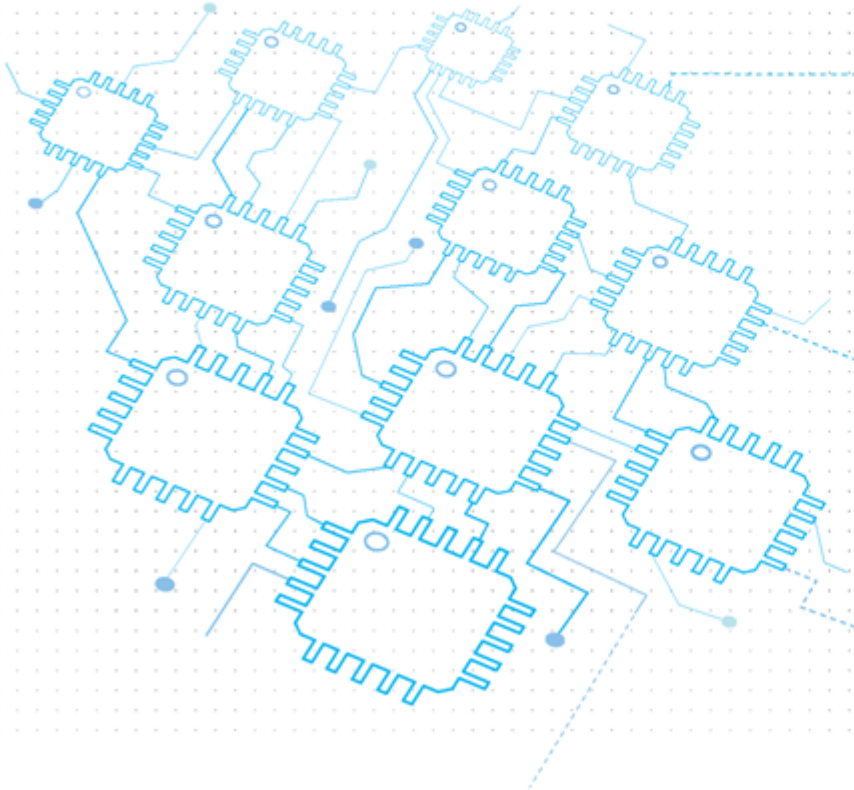
Academy of Sciences of the Czech Republic
Institute of Information Theory and Automation AS CR, v.v.i.



department of signal processing

Department of Signal Processing

ÚTIA AVČR v.v.i.

http://zs.utia.cas.cz

Presentace Plzeň 6.12.2011

Overview of the Department

- **History**
  - Established in 2000 with the vision: Research and design parallel signal processing algorithms and implement them as hardware modules for FPGAs and embedded CPUs.
- **People, and expected structure (from 2012)**
  - Ing. Martin Daněk PhD. (1.0); deputy head of department
    - Ing. Roman Bartosinski PhD.(1.0);
    - Ing. Lukáš Kohout (1.0);
    - Ing. Jaroslav Sýkora (1.0);
  - Ing. Zdeněk Pohl PhD. (1.0);
    - Ing. Tomáš Mazanec (1.0);
  - Ing. Jiří Kadlec CSc. (1.0); head of department
    - Ing. Radim Matulík (1.0);
    - Mgr. Milada Kadlecová (1.0).

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Department of Signal Processing

- **Topics**
  - adaptive signal processing; digital communication algorithms;
  - processor micro-architectures; embedded systems architectures;
  - FPGA-based prototyping.
- **Strengths**
  - Algorithmic research, architecture design and implementations in Field Programmable Gate Arrays (FPGA).
  - Strong track record of participation in the EU framework program ICT collaborative research (2005-09: 2x STREP, 1x IP, 5x SSA).
  - Successful cooperation with a number of industrial customers (2005-09: 1x Italy,1x USA, 1x UK, 3x CZ).
  - Unique expertise in placement and routing algorithms for a commercial FPGA chip, reaching up to bit-stream generation.
  - The highest involvement in the EU technology-oriented ARTEMIS JU projects in the ASCR.

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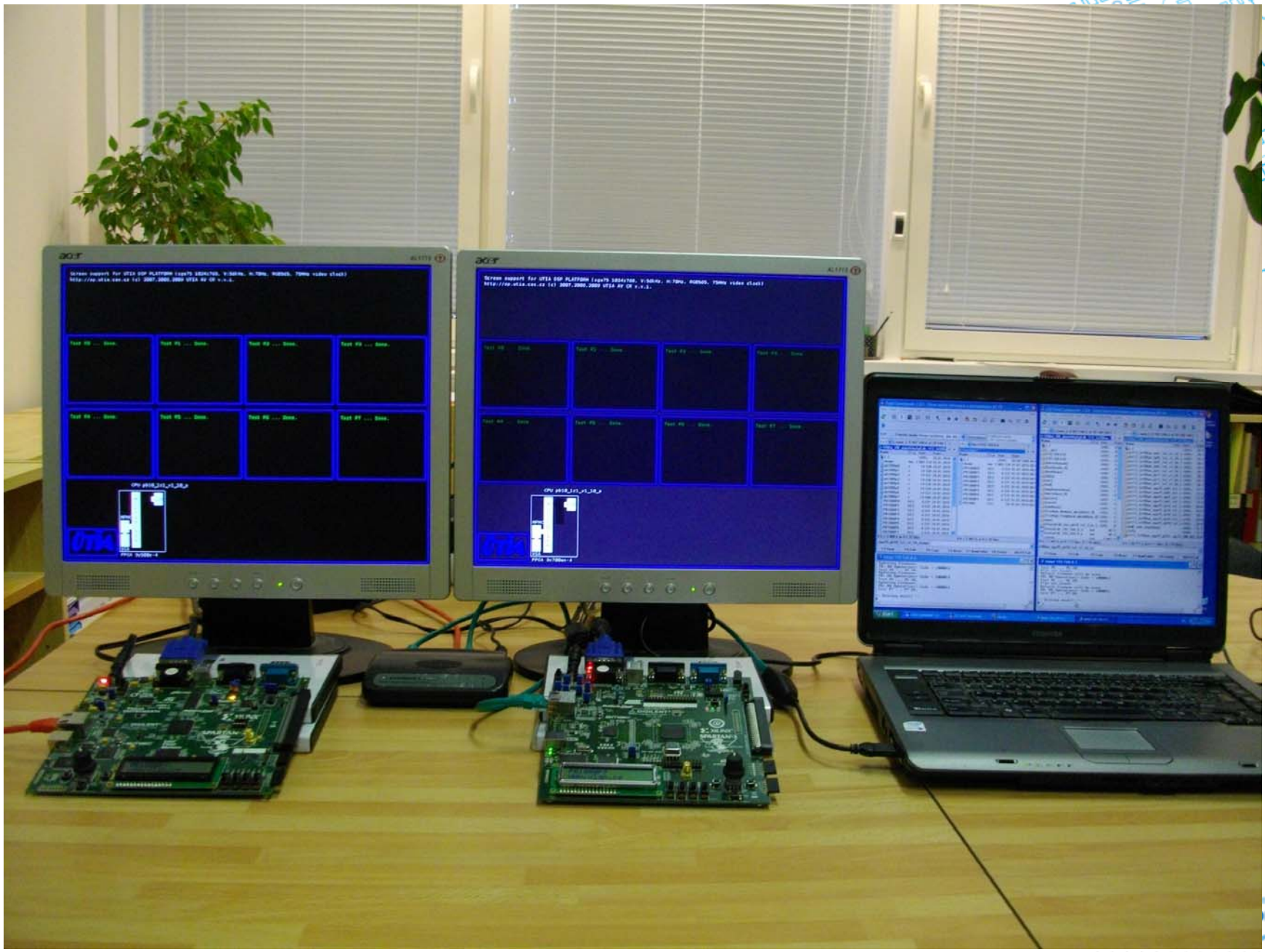
National Projects 2005-2011

	Adapt. DSP	Digital Com. Alg.	Proc Micro Arch.	Emb. Syst. Arch.	FPGA based Protot.	FPGA techn ology	SSA	National Program in CZ
CAK 2	X		X	X	X			Apl. Res. Centers 1M
RETAC					X	X		NPV1 PP2
RIPAC				X	X			NPV1 TP2
SESAP				X	X			NPV1 TP2
ORFEUS		X			X			NPV1 TP2
ADSL	X	X						NPV1 TP2
VLAM			X	X	X			NPV2
OKO-ICT 2x							X	EUPRO
RICARDO s.r.o.				X	X			Ind. Cont. Research
ERA a.s.	X	X			X			Ind. Cont. Research

International Projects 2005-2011

	Adapt. DSP	Digital Com. Alg.	Proc Micro Arch.	Emb. Syst. Arch.	FPGA based Protot.	FPGA techn ology	SSA	EU Frame-work. Pr.
IST World							X	FP6
Idealist (4x)							X	FP6,FP7
Cosine (2x)							X	FP6,FP7
XML-FED					X			EUREKA
AETHER				X	X	X		FP6
Apple-CORE	X		X	X	X			FP7
SCALOPES	X	X		X	X			ARTEMIS JU
SMECY	X		X	X	X			ARTEMIS JU
ATMEL Corp.				X	X	X		Ind. Cont. Research

EdkDSP 3s500e & 3s700an & Petalinux



Vision and Opportunities

Vision

- Our vision is to develop into a strong player in the area of advanced computing architectures for application specific signal processing.

Opportunities (from early 2012 …)

- Use of our EdkDSP embedded platform with soft-processor cores and embedded operating systems with custom parallel hardware accelerators as an effective path to increased design productivity due to reuse.

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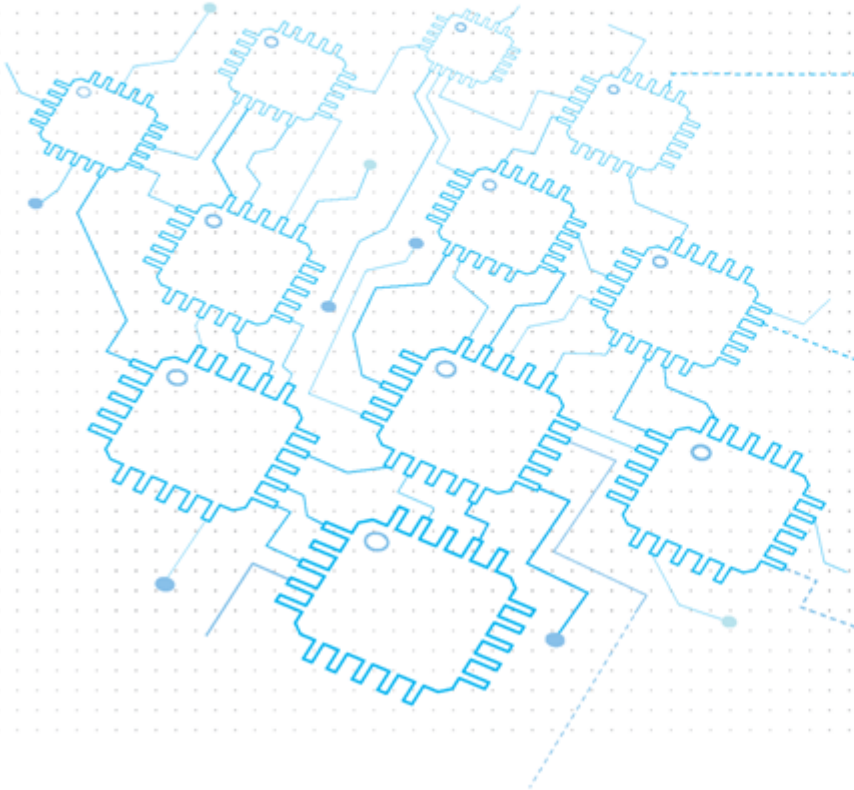

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Floating Point accelerators in FPGA EdkDSP Platform

Jiří Kadlec,
ÚTIA Prague, CZ
http://zs.utia.cas.cz

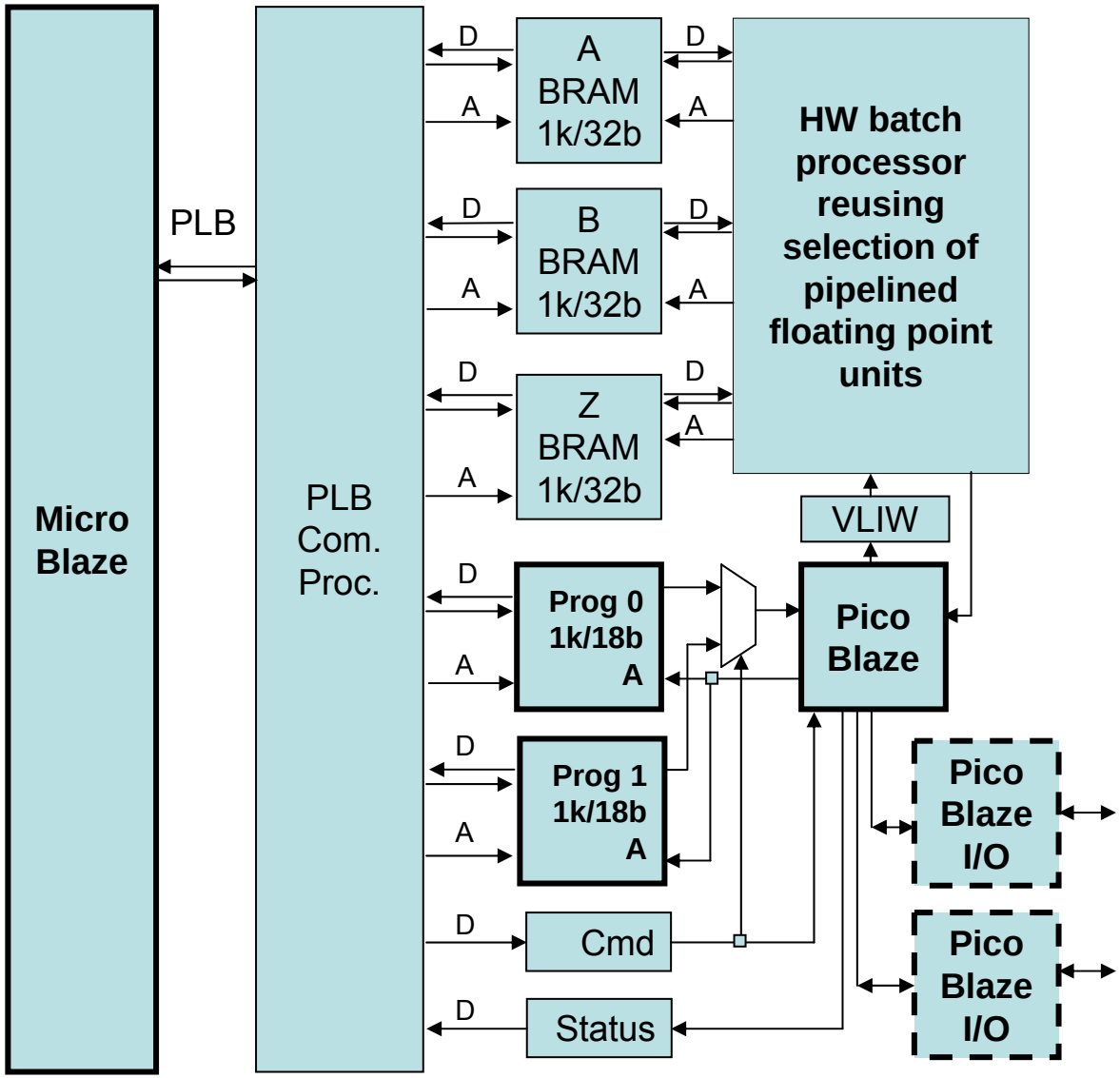
Plzeň 6.12.2011

Motivation

- To implement an accelerator for DSP computing that would
  - Maximize the utilization of pipelined (floating-point) units.
  - Cover a whole class of problems rather than one specific problem.
  - Reuse the datapath and element counters.
  - Use a simple sequencer to reduce HW muxes in the datapath.

- Robust design and validation methodology using the existing affordable Xilinx design tools.

Runtime re-programming: Firmware can be changed on the fly



- Swap of PicoBlaze firmware can be done in few clock cycles
- Reprogram while executing

- LEDs, SWs, BTNs
- LCD (2 lines ascii)
- Rotary encoder
- Serial/Par. FLASH
- ADC/DAC controller
- PWM

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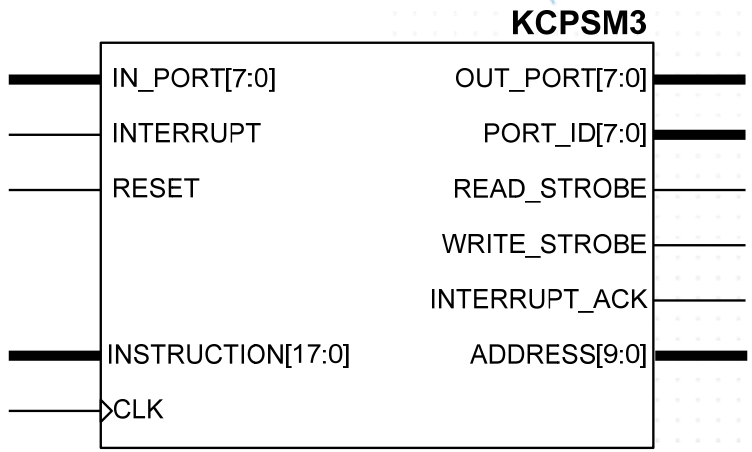
PicoBlaze – Introduction

- KCPSM3 – (K)constant Coded Programmable State Machine
- 8-bit microcontroller by Ken Chapman, Xilinx
- Soft-core for Xilinx Spartan-3(E), Virtex-II and Virtex-II PRO
- 96 Spartan-3 slices (10% of the XC3S100E)
- 50MIPS@100MHz
- Development tools: Mediatronix pBlazeIDE, kpicosim, PCCOMP

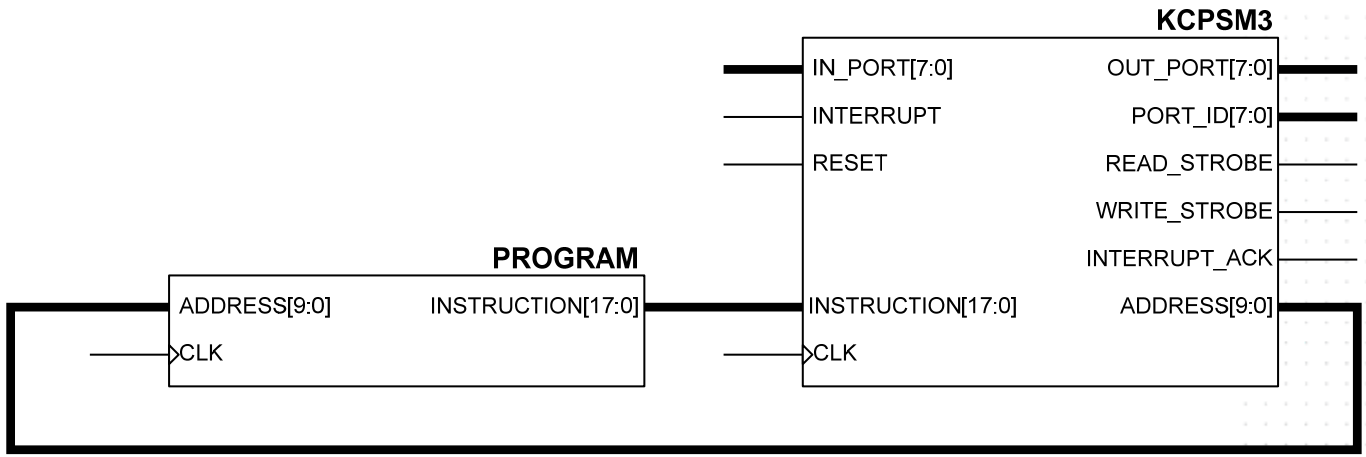
PicoBlaze – Features

- RISC, Harvard architecture
- 16 general purpose registers
- 64B internal scratch pad memory
- 256 input and 256 output ports
- Single INTERRUPT input
- 31-level deep HW stack
- Program in BlockRAM
- Program length up to 1024 instructions

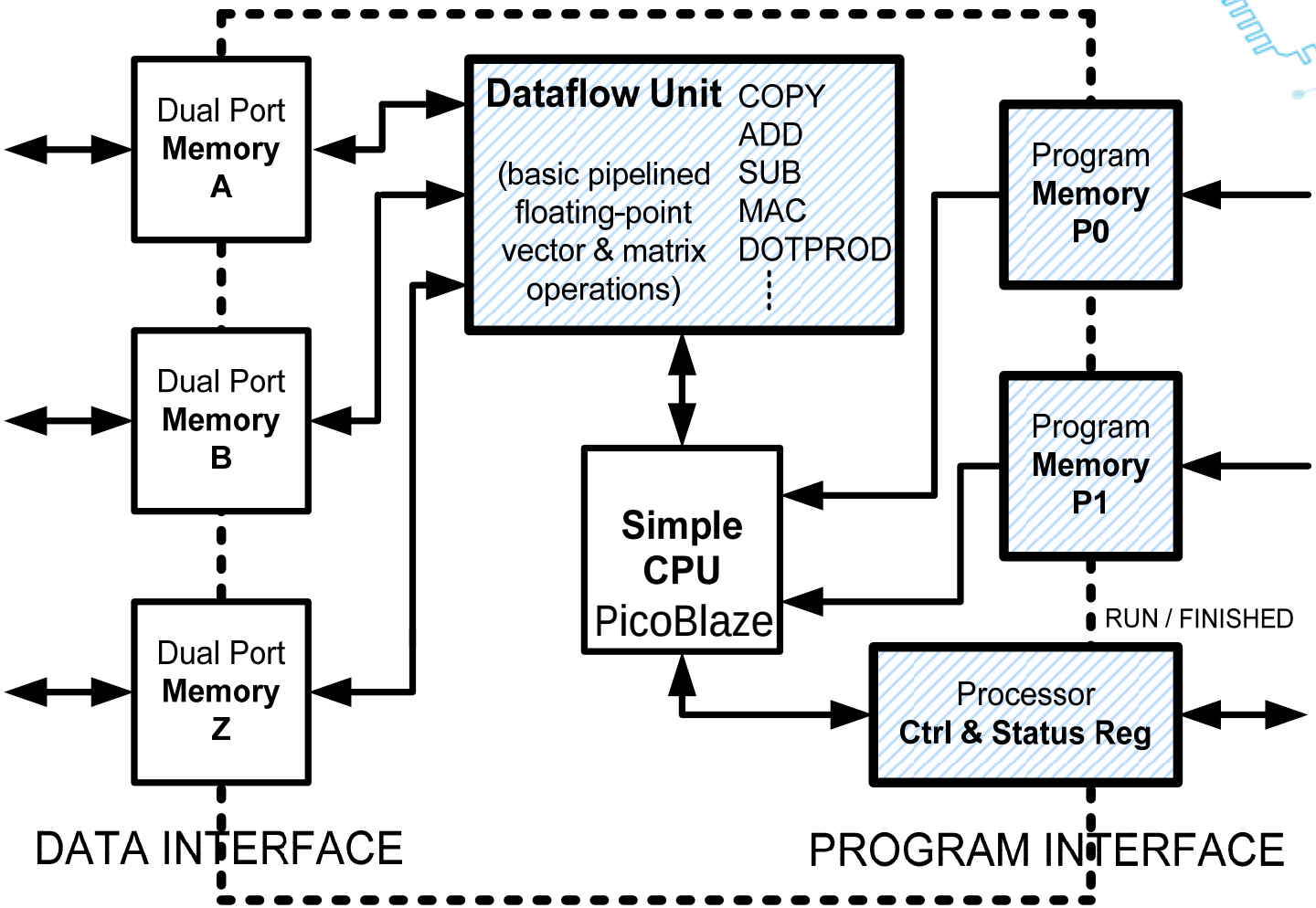


PicoBlaze – Instruction Memory

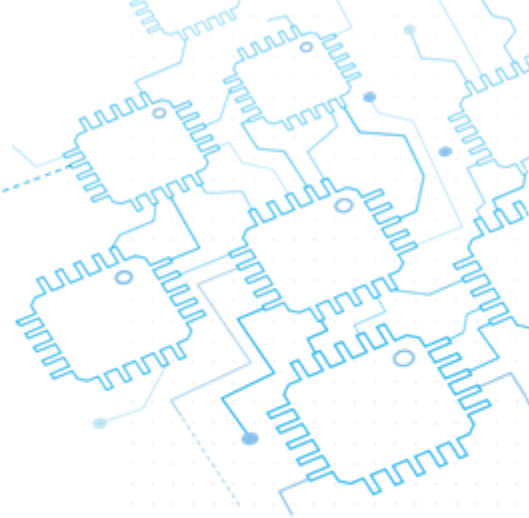
- 18Kbit BlockRAM instantiated in the design
- BlockRAM content defined by the assembler
- One port of the BlockRAM is used for the PicoBlaze core, the second port is not used



Basic Computing Element (BCE)



Vector operations supported by HW
1x FP Add and 1x FP Mult unit



- HW version
- COPY vector `a[i] = z[j];` `a[i] = b[j];`
  `b[i] = z[j];` `b[i] = a[j];`

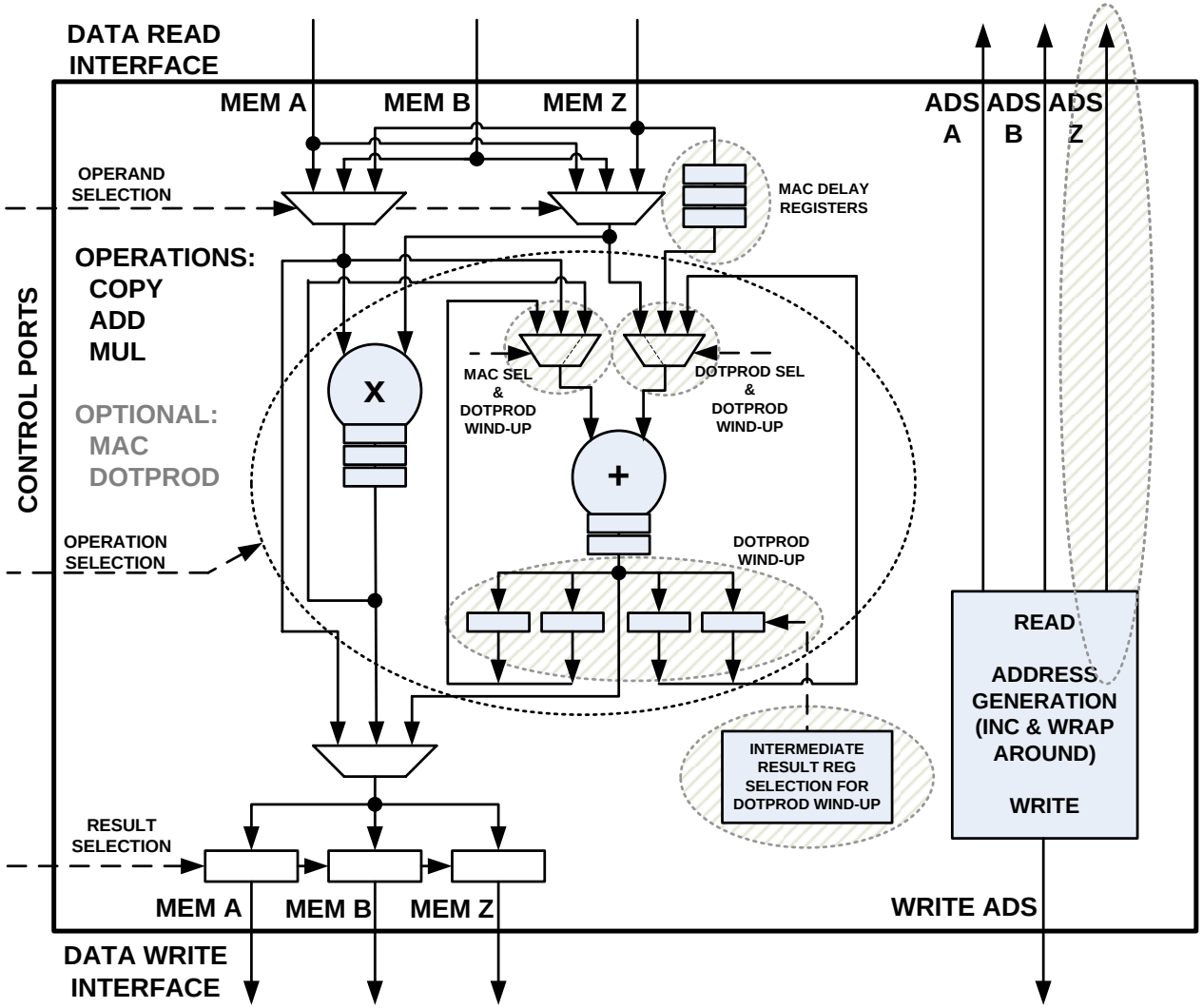
- ADD vectors `z[i] = a[j] + b[k]; a[i] = b[j] + z[k]; b[i] = a[j] + z[k];`
- SUB vectors `z[i] = a[j] - b[k]; a[i] = b[j] - z[k]; b[i] = a[j] - z[k];`
- MULT vectors `z[i] = a[j] * b[k]; a[i] = b[j] * z[k]; b[i] = a[j] * z[k];`

- MAC `z[i] = z[i] + a[j] * b[k]; z[i] = z[i] - a[j] * b[k];`

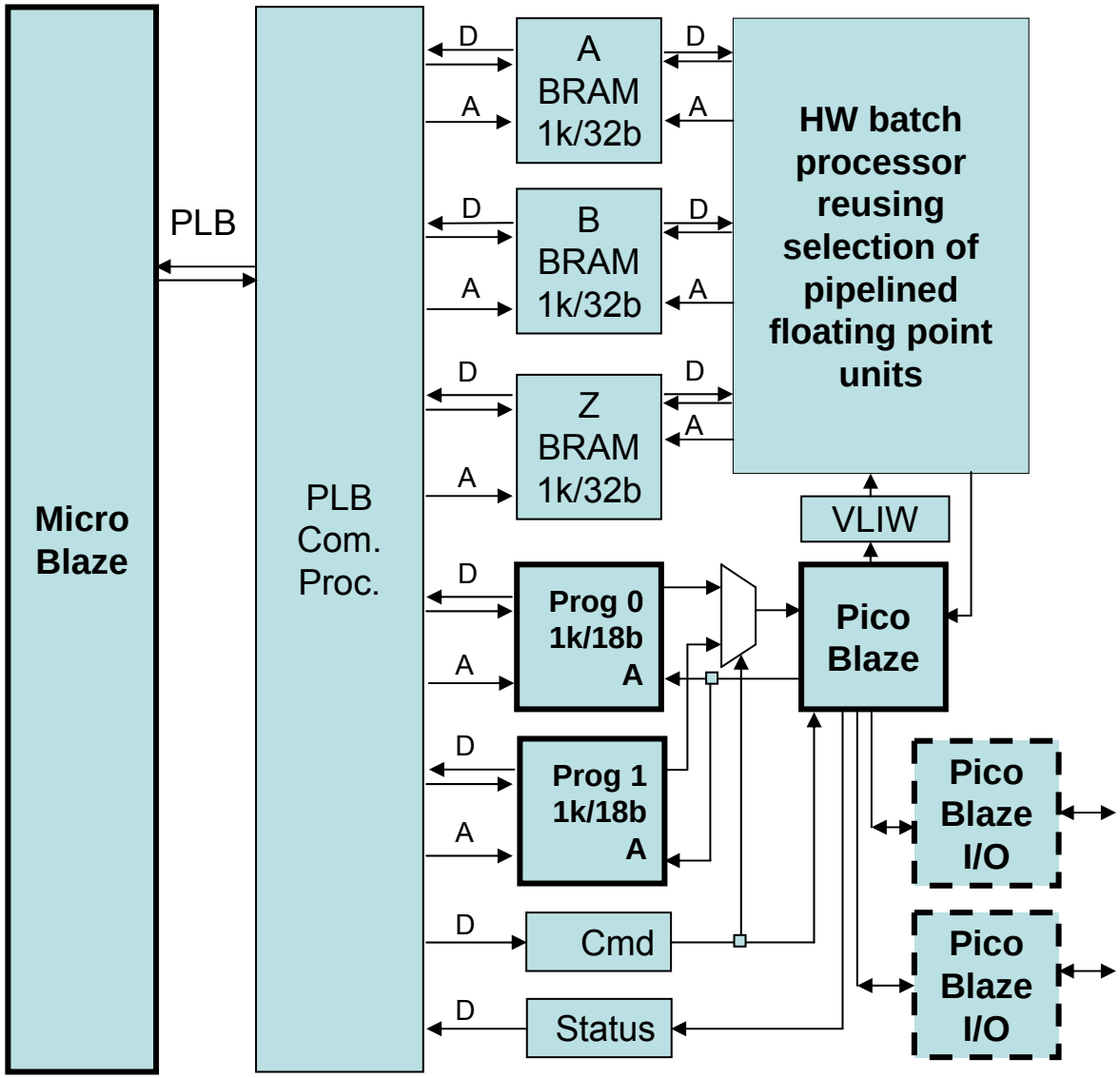
- DOT PRODUCT `z[k] = a'[i..i+nn] * b[i..i+nn];`

- Special …

Data-Flow Unit (DFU)



Runtime re-programming: Firmware can be changed on the fly



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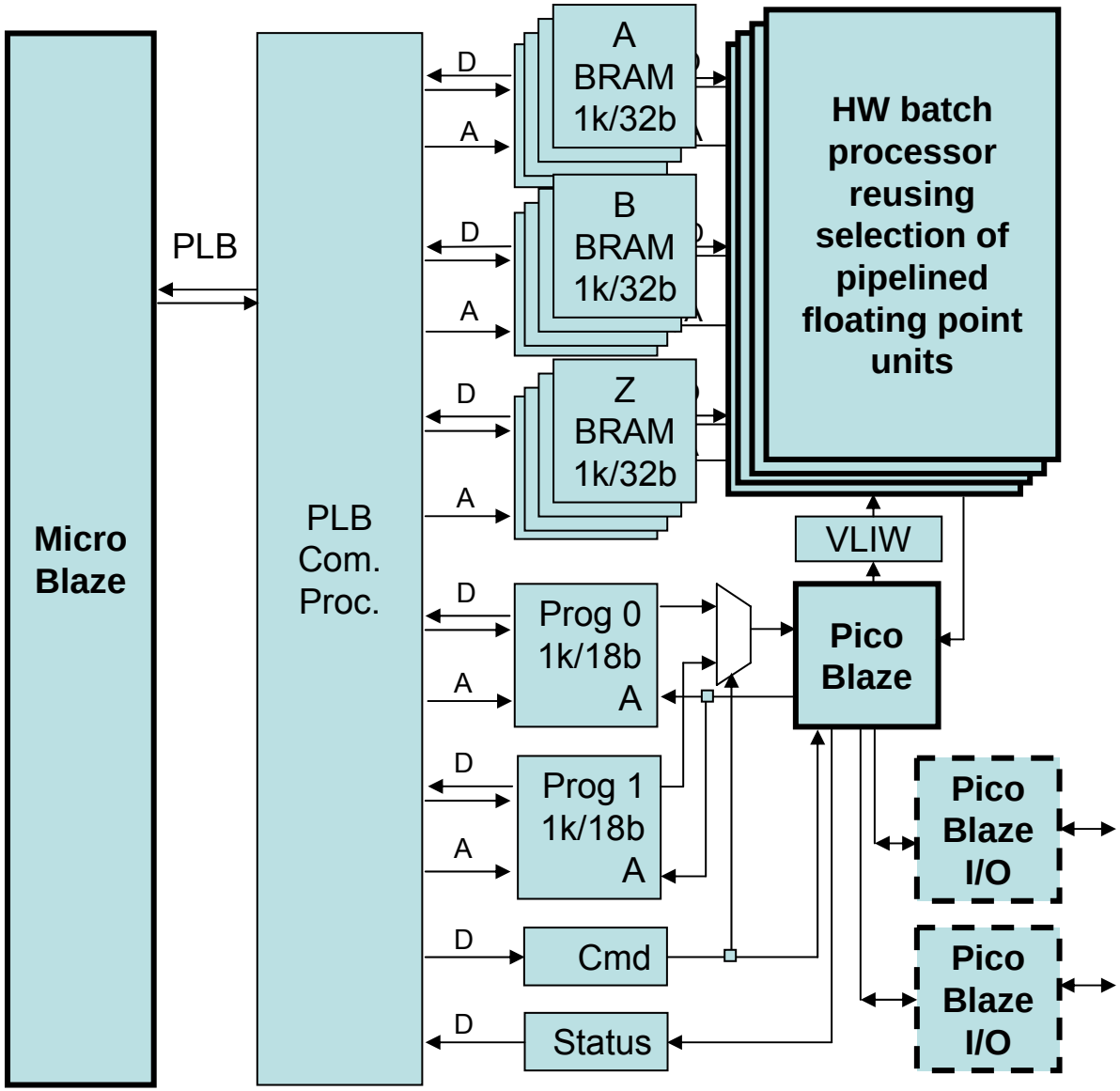
Example of accelerator with four SIMD FP data paths



Area: 40 - 50% of Xilinx Spartan FPGA 3sd1800a

Power: 0,4 - 0,6 W

Performance peak: 600 MFLOPs
Performance typical: 200 MFLOPs (Application specific)

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SW Tool Chain for EdkDSP

- Single FPGA without OS:
  - MicroBlaze: C: GCC (WinXP/Linux)
  - PicoBlaze: ASM: kcpsm3(WinXP), C: PCCOM (WinXP)
- Multiple FPGA, 100 Mb Ethernet, uCLinux (no MMU)
  - MicroBlaze: C: GCC (Linux) C++: G++ (Linux)
  - PicoBlaze: ASM: kcpsm3(WinXP), C: PCCOM (WinXP)
  - OS: Petalogix Petalinux-v0.40-final
- Board support for Xilinx FPGA starter kits (ISE/EDK 13.3):
  - 3S1600E, 3S500E, 3S700AN
  - 3SD1800A, 3SD3400A
  - 6SLX16, 6SLX45T

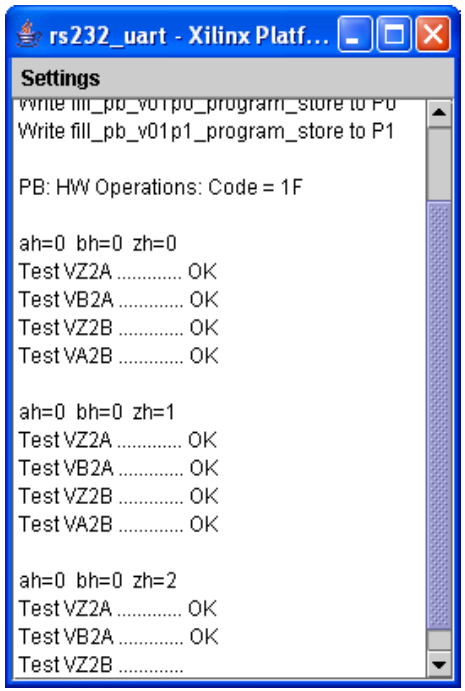
Current HW Simulation/ Design Chain

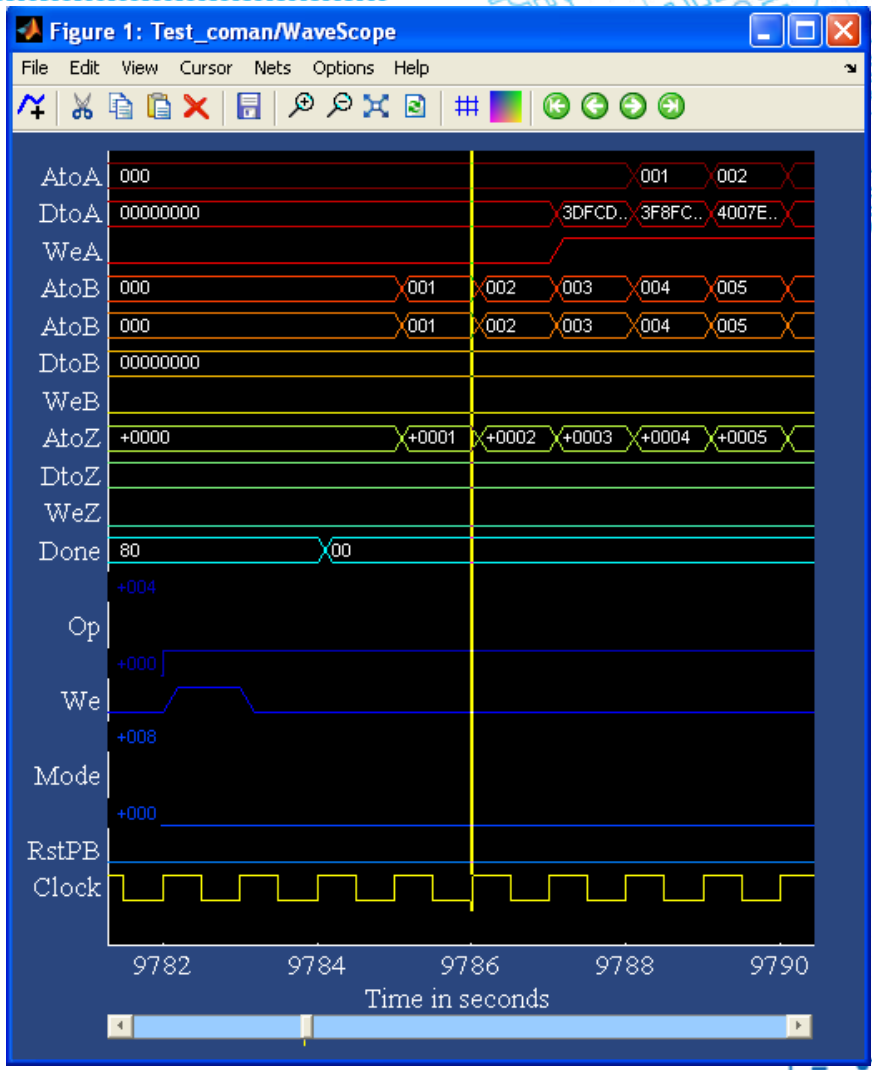
- Simulation and Development of Accelerators:
  - Mathworks Matalb/Simulink (2010b)
  - Xilinx System Generator (13.3)
  - Ethernet P2P, transaction based HW/SW co-simulation:
    - Free running MicroBlaze SW +
    - Single EdkDSP Accelerator HW in Simulink
- HDL generation
  - Accelerators are exported to EDK as netlist PLB pcores
  - Tools: Xilinx XPS 13.3 SDK 13.3 EDK 13.3

Simulation

Xilinx System Generator

- HW co-simulation
  XSG 13.3
- Virtual platform
  XSG 13.3

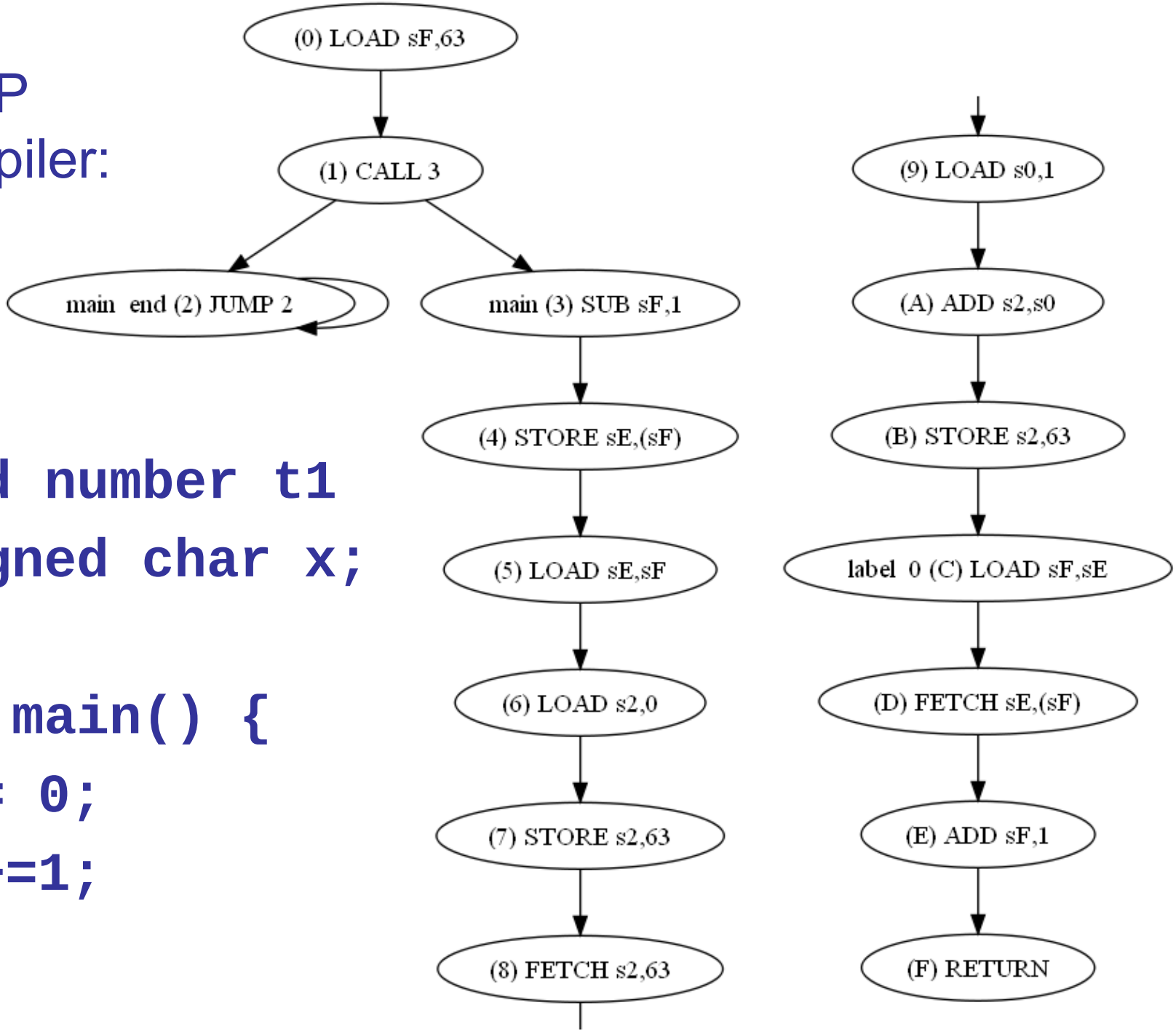




EdkDSP SW/HW Back End Tools

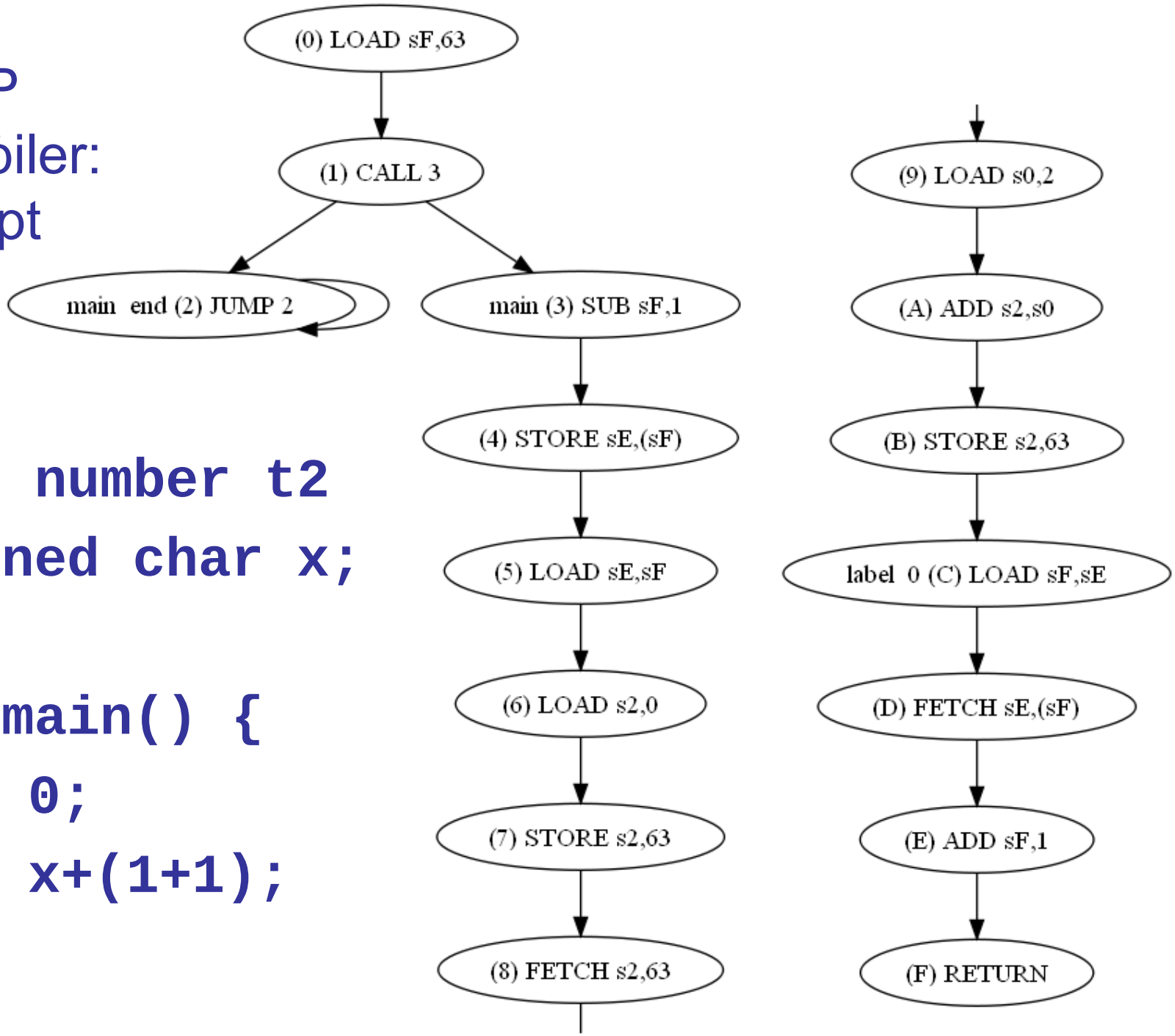
- ASSEMBLER for PicoBlaze Accelerators with FP data paths:
  - Executable on PC (WinXP/Linux)
  - Executable directly on the FPGA (MicroBlaze with uCLinux)
- C COMPILER for PicoBlaze Accelerators with FP data paths:
  - Executable on PC (WinXP/Linux)
  - Executable directly on the FPGA (MicroBlaze with uCLinux)
- Interface/Integration/Interaction with Front End Tools
- Dedicated Support for Stream Processing Video Appl.
- Board support:
  - 3S500E, 3S700AN, 3S1600E, 3SD1800A, 3SD3400A - vsk
  - 6SLX16, 6SLX45T, 6SLX110T - vsk

EdkDSP C Compiler: uchar




```
//add number t1
unsigned char x;

void main() {
  x = 0;
  x +=1;
}
```

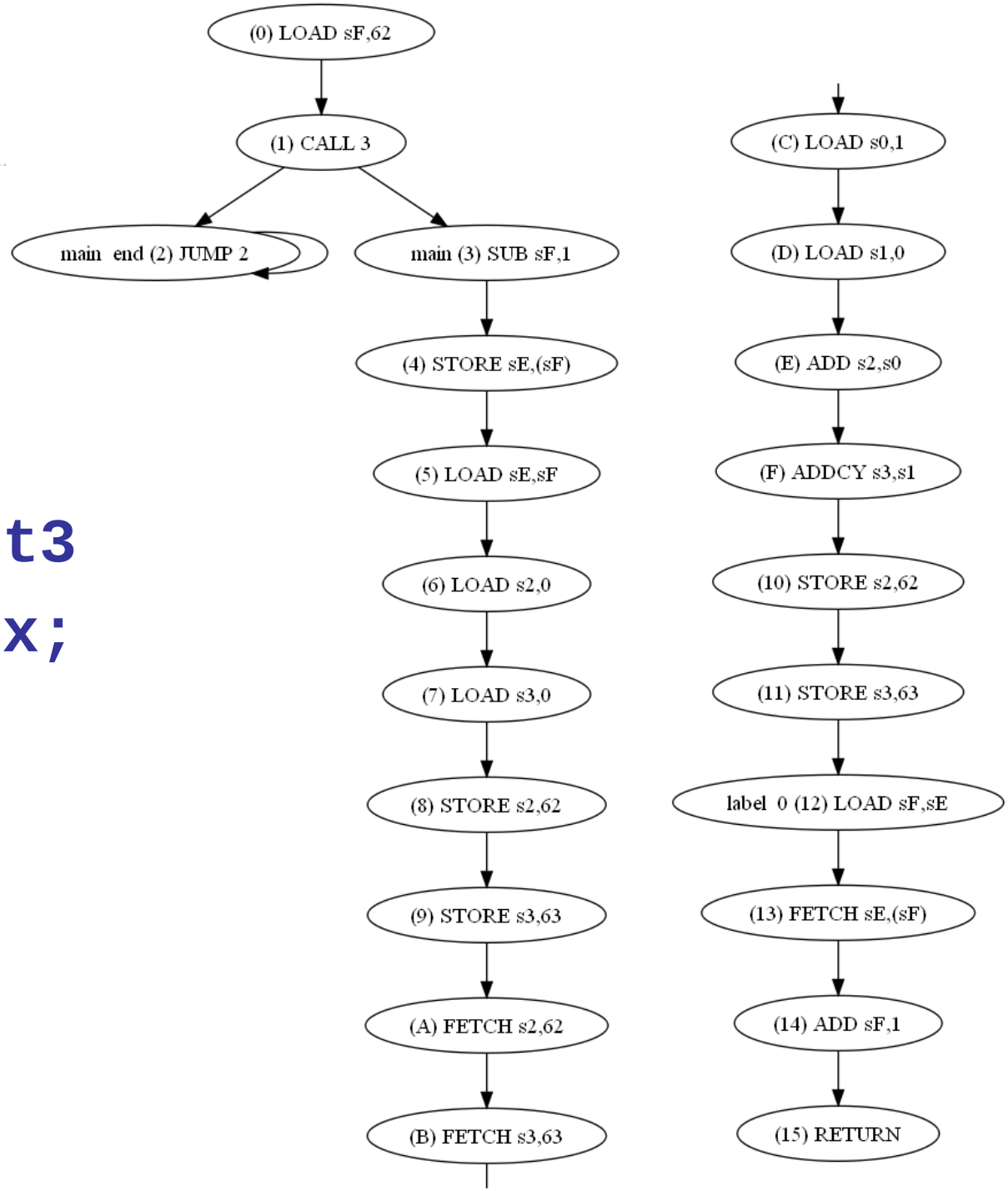
EdkDSP
C Compiler:
uchar opt




```
//add number t2
unsigned char x;

void main() {
  x = 0;
  x = x+(1+1);
}
```

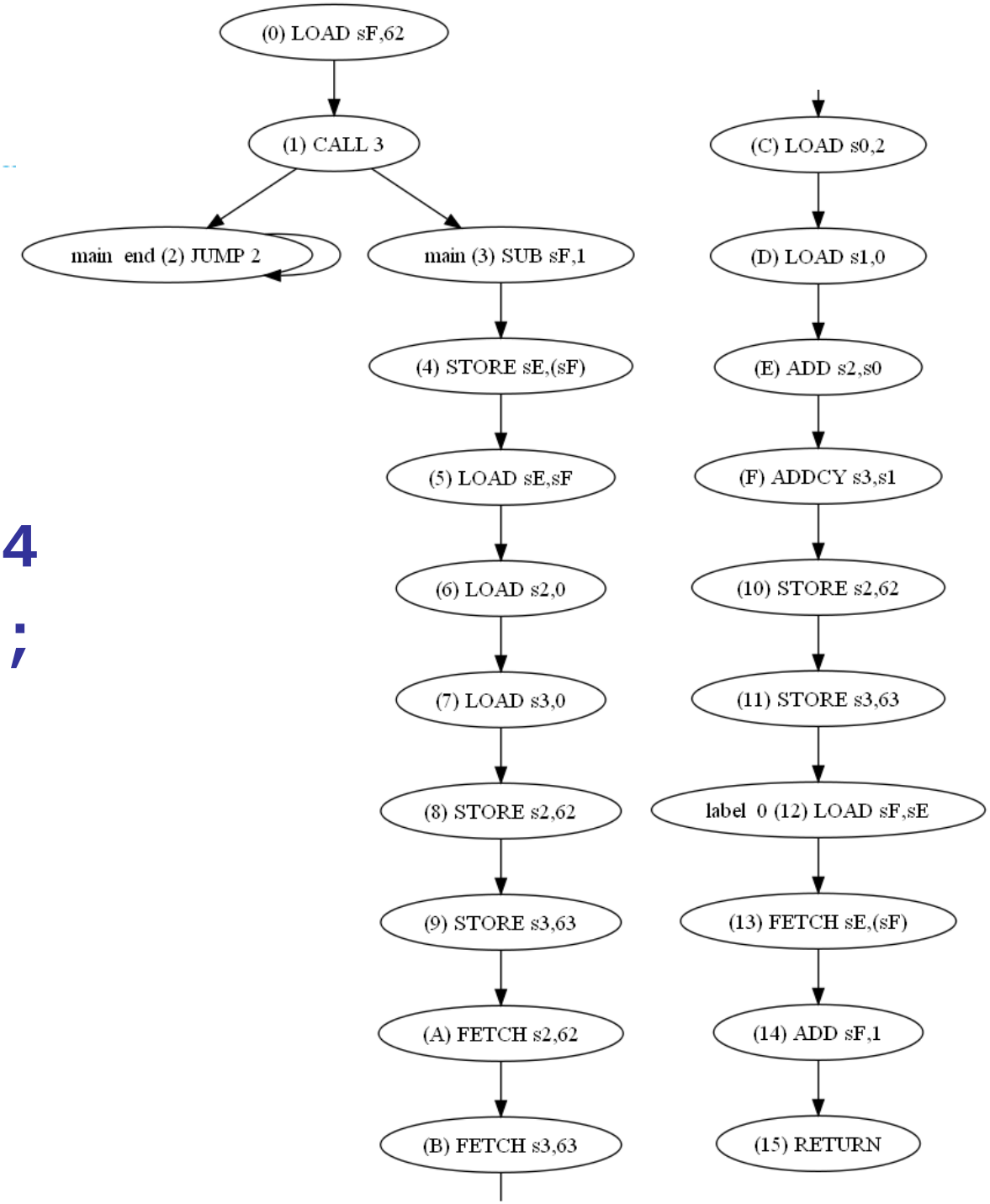
EdkDSP C Compiler: uint

```
//add number t3
unsigned int x;

void main() {
  x = 0;
  x +=1;
}
```

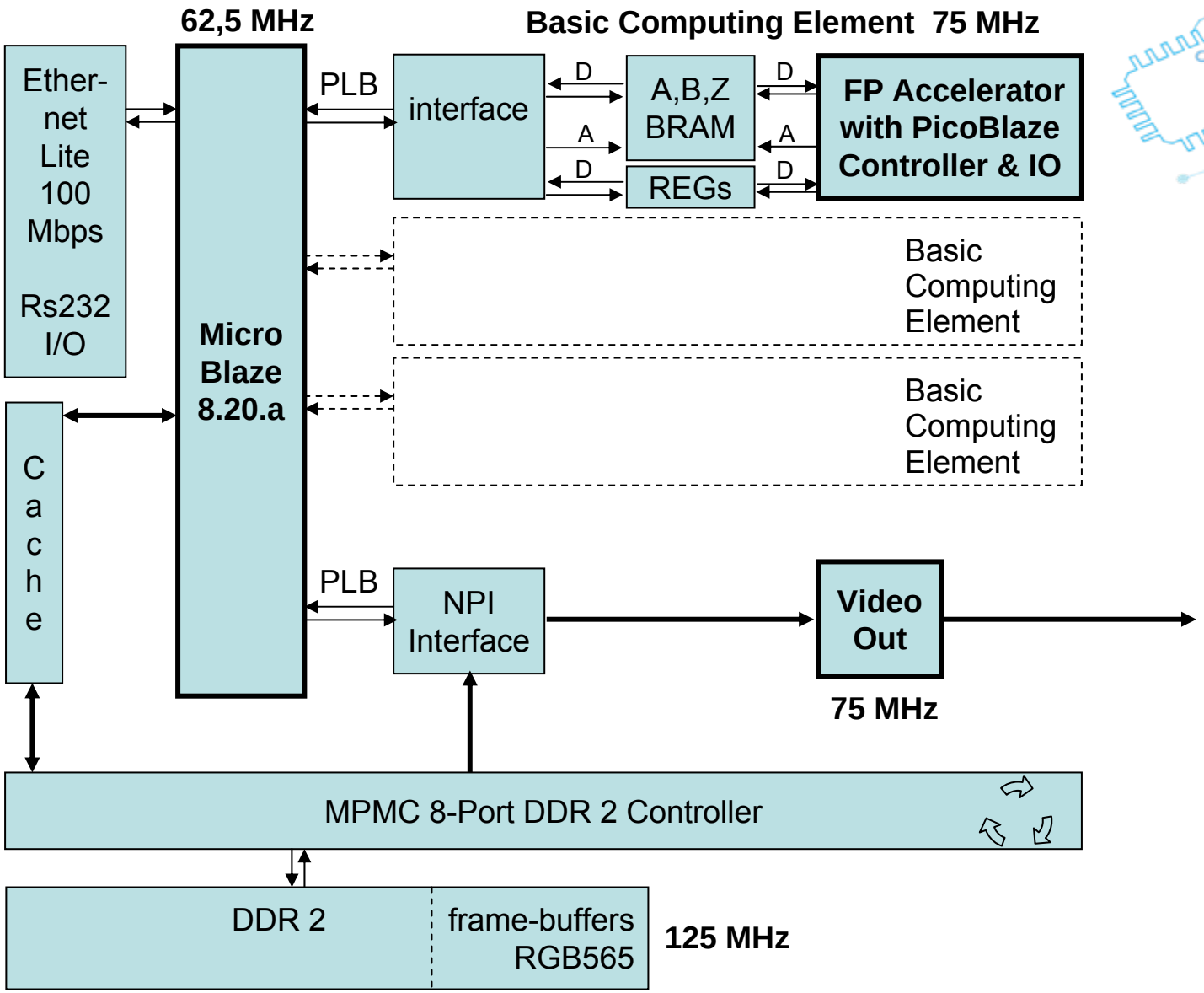


EdkDSP
C Compiler:
uint opt

```
//add number t4
unsigned int x;

void main() {
  x = 0;
  x = x+(1+1);
}
```



EdkDSP Batch processing & Visualisation



Spartan 3 Xilinx boards supported by UTIA:

3s500e
3s1600e
3s700an
3sd1800a
3sd3400a

RGB565 1024x768 70Hz

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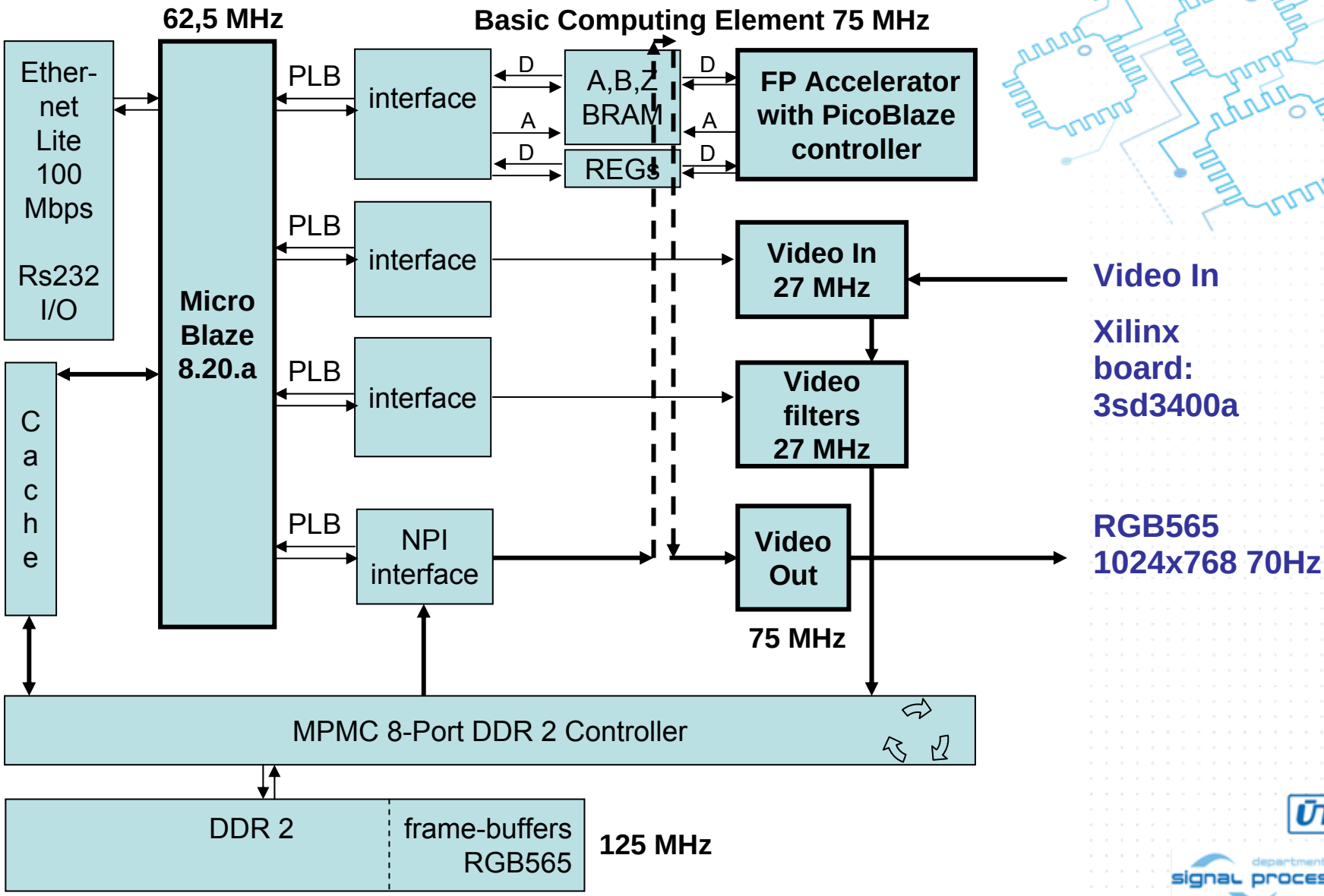
EdkDSP Stream Processing



Demos and Opportunities

- **Opportunities**
  - Use in education in your labs (5x xc3s1600e …)
  - Use in industrial automation and data processing
  - Strategy towards FP7, Artemis JU and Eniac JU
  - Strategy towards GACR / TACR
  - Direct participation in industrial contracts